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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,701	08/05/2003	Mitsuhide Kato	36856.1102	6786

54066 7590 09/07/2005

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,701	KATO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-12 and 17-21* is/are rejected.

7)☒ Claim(s) *5,7 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0803//05 Aug 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 11 (both of them) and Claims 12-20 are objected to because of the following informalities:

There are **two** distinct claims numbered as Claim 11. The Examiner will refer to the second Claim 11 (the one that is dependent from Claim 9) as Claim 12', and all the subsequent claims will be referenced as 13'-21'. Accordingly, there are **21 claims** in the instant Application: Claims 1-11 plus the second Claim 11 through 20, renumbered for examination purposes as 12'-21'. The Applicant needs to renumber the claims properly in accordance with 37 CFR § 1.126 and either cancel a claim (Applicant payed for only 20 claims) or keep the 21 claims after renumbering and submit payment for the extra dependent Claim 21' and any other additional claims responsive to the present Office Action. Please be aware that in Claims 12'-21' the indicated claim dependencies must also be corrected.

2. Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Hirasawa et al. (US 6,555,763 B1)

Ehman et al. (US 6,021,050)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 6, 8-11, 12' and 17'-19' are rejected under 35 U.S.C. 102(e) as being anticipated by Hirasawa et al.

As to Claim 1, Hirasawa et al. discloses: a laminated block (Figs. 3A-E and 6) including a plurality of electrically insulating layers (layers 21 in the embodiment of Figs. 3A-E, and layers 2, 3 and 1b in the embodiment of Fig. 6; col.3: 8-12, col.4: 4-9 and col.5: 24-35) and an internal conductor film 1a disposed between the insulating layers 3 and 1b (Fig. 6) laminated together in a thickness direction of the laminated block (Figs. 3D, 3E and 6; col.5: 28-30); an external conductor film 4 disposed on an exposed surface of the laminated block (i.e., the upper surface of insulating layer 3; Figs. 3D and 6); and an additional conductor film 4 (Figs. 3D and 6) which is at the same electrical potential as the external conductor film 4 (i.e., ground; col.3: 8-11) and which is arranged along a specific interface between the insulating layers 2 and 3 such that the additional conductor film 4 faces external conductor film 4 (Fig. 6).

As to Claim 2, Hirasawa et al. further discloses, in Fig. 6, only one of the insulating layers (i.e., layer 3) is interposed between the additional conductor film 4 and the external conductor film 4.

As to Claim 3, Hirasawa et al. further discloses the thickness of the insulating layer 3 (layer 21 in the lamination step disclosed in Fig. 3A) between the additional conductor film 4 and the external conductor film 4 is about 50 μm; i.e., ranges from about 10 μm to about 150 μm (col.4: 1-4).

As to Claim 4, Hirasawa et al. further discloses the thickness of the insulating layer 3 (layer 21 in the lamination step disclosed in Fig. 3A) between the additional conductor film 4 and the external conductor film 4 is about 50 μm; i.e., ranges from about 25 μm to about 150 μm (col.4: 1-4).

As to Claim 6, Hirasawa et al. further discloses the additional conductor film 4 and the external conductor film 4 are electrically connected to each other through a via-hole conductor 5 (Fig. 6; col.3: 9-11).

As to Claim 8, a DC bias applied between the external conductor film 4 and the internal conductor film 1a (col.5: col.5: 43-46).

As to Claim 9, Hirasawa et al. further discloses the laminated block includes a first main surface (top surface of insulating layer 3) and a second main surface (bottom surface of insulating layer 1b) facing the first main surface, and external conductor film 4 is disposed on the first main surface (Fig. 6).

As to Claim 10, Hirasawa et al. further discloses a chip component (semiconductor chip 9) mounted on the first main surface, wherein external conductor

film 4 is arranged to establish an electrical connection with chip component 9 (Fig. 2 and col.3: 30-46).

As to Claim 11, Hirasawa et al. further discloses the chip component 9 is an integrated circuit; i.e., a semiconductor chip (col.3: 31-32).

As to Claim 12' (wrongly-numbered Claim 11), Hirasawa et al. further discloses external conductor film 4 is arranged to establish an electrical connection with a board (i.e., a motherboard) on which the laminated electronic component is mounted (Fig. 2; col.3: 38-46).

As to Claim 17' (wrongly-numbered Claim 16), Hirasawa et al. further discloses internal conductor film 1a defines a ground potential (col.5: 43-44).

As to Claim 18' (wrongly-numbered Claim 17), Hirasawa et al. further discloses a plurality of internal conductors and via-hole conductors which are arranged to provide wiring patterns, not shown (col.2: 67-col.3: 7).

As to Claim 19' (wrongly-numbered Claim 18), Hirasawa et al. further discloses the plurality of internal conductors and via-hole conductors are disposed within the laminated block (Figs. 1 and 6; col.2: 67-col.3: 7).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 20' and 21' are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirasawa et al. in view of Ehman et al.

As to Claims 20' and 21' (wrongly-numbered Claims 19 and 20):

I. Hirasawa et al. discloses a laminate electronic component (Fig. 6) which can have more layers and circuitry than is disclosed (col.2: 67-col.3: 7) but does not teach the inclusion of resistor films for defining resistors disposed on or within the laminated block.

II. Ehman et al. discloses a laminated block that comprises resistor films on and within the laminated block 10 for defining resistors 26 in order to provide the resistor functionality in the laminate block 10 such that the cost and space required on the laminate block 10 is reduced by including printed resistors (among other passive printed elements) within the laminated block 10 (Fig. 1; col.1: 12-18 and 42-47; col.3: 13-25 and 46-53).

III. Since Hirasawa et al. and Ehman et al. disclose a laminated block with multilayered circuitry, then the inclusion of printed resistors disposed within the laminated block for defining resistors to perform required circuit functions, wherein the printed resistors are in the form of resistor films that enable a high density of circuitry without requiring as much laminated block space as discrete resistors do, and enable a lower cost high density laminate block, as taught by Ehman et al., would have been readily recognized in the pertinent laminated block art of Hirasawa et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the laminated block of Hirasawa et al. with printed resistor films disposed within the laminated block to provide the functional circuitry for the application without increasing the size and cost of the laminated block, as taught by Ehman et al.

Allowable Subject Matter

9. Claims 5, 7, 13'-15' and 16' are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Kitazawa et al. (US 6,057,600) discloses a laminate block comprising vias 12a,b and layers 3 and 7, all at the same potential (Fig. 1; col.9: 34-51).

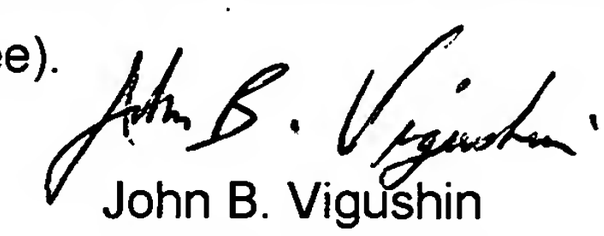
b) Van Dyke et al. (US 6,657,130 B1) discloses equipotential layers (col.5 : 57-col.6 : 3; col.6: 27-35) in a ceramic laminate block (col.6: 47-49).

c) Ohsaka (US 6,800,814 B2) discloses equipotential layers (col.14: 39-42).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
September 04, 2005